Remarks

The Office Action dated October 16, 2001, has been obtained and carefully noted. The following remarks are submitted as a full and complete response thereto.

No amendments have been made to the present application, and therefore no new matter has been added. Accordingly, claims 1-15 are pending in the present application and are respectfully submitted for consideration.

Claims 1-4, 6-12, 14 and 15 were rejected under 35 U.S.C. § 102(b) as being anticipated by Applicant's admitted prior art ("AAPA"). Applicant respectfully submits that each of claims 1-4, 6-12, 14 and 15 recites subject matter that is neither disclosed nor suggested by AAPA.

Claim 1 recites a signal processing circuit having a decision feedback equalizer for waveform-equalizing a digital signal in accordance with a clock signal and generating the waveform-equalized digital signal, and a timing recovery PLL, connected to the decision feedback equalizer, for generating the clock signal, the clock signal having a phase which is substantially coincident with the phase of the digital signal, based on the phase difference between the digital signal and the clock signal, and supplying the clock signal to the decision feedback equalizer. The decision feedback equalizer includes, a prefilter for filtering the digital signal and generating a filtered digital signal, a decision circuit, connected to the prefilter, for adding a feedback signal and the filtered digital signal and generating an addition signal, and for analyzing the addition signal in accordance with predetermined criteria to generate a decision signal, and a shift register, connected to the decision circuit, for sampling the decision signal in accordance with the clock signal and storing sampling data. The sampling data stored

in the shift register is output from the shift register as the waveform-equalized digital signal. In addition, the decision feedback equalizer includes a feedback filter, connected to the shift register, for receiving the sampling data and generating the feedback signal using the sampling data, and a loop control circuit for monitoring the filtered digital signal and the feedback signal and controlling a feedback loop formed by the decision circuit, the shift register, and the feedback filter based on a monitoring result.

Claim 9 recites, in a signal processor, a feedback control method having the steps of filtering a digital signal to generate a filtered digital signal, adding a feedback signal and the filtered digital signal to generate the addition signal, and analyzing the addition signal in accordance with predetermined criteria to generate a decision signal. In addition, the steps include sampling the decision signal in accordance with a clock signal to store sampling data in a shift register; generating the feedback signal using the sampling data stored in the shift register, and generating the clock signal, which is substantially coincident with the phase of the digital signal, based on a phase difference between the digital signal and the clock signal. Furthermore, the steps includes monitoring the filtered digital signal and the feedback signal, and selecting whether the feedback signal is fed back to the step of generating the addition signal based on a monitoring result.

Claim 15 recites in a signal processor, a feedback control method having the steps of filtering a digital signal to generate a filtered digital signal, adding a feedback signal and the filtered digital signal to generate the addition signal, analyzing the addition signal in accordance with predetermined criteria to generate a decision signal,

sampling the decision signal in accordance with a clock signal to store sampling data in a shift register, generating the feedback signal using the sampling data stored in the shift register, and calculating a first phase difference between the digital signal and the clock signal using the decision signal and a first reference signal. The first reference signal has a first predetermined value at preset control point of the filtered digital signal. In addition, the steps include generating the clock signal having a phase which is substantially coincident with the phase of the digital signal, based on a first phase difference, determining whether the first phase difference is within a predetermined range, feeding back the feedback signal to the step of generating the addition signal when the first phase difference is within the predetermined range, calculating a second phase difference between the digital signal and the clock signal using the decision signal and a second reference signal, wherein the second reference signal has a second predetermined value at the preset control point preset of the decision signal, and regenerating the clock signal having a phase which is substantially coincident with the phase of the digital signal, based on the second phase difference.

Accordingly, at least one of the essential features of the present invention with respect to claim 1 is "a loop control circuit for monitoring the filtered digital signal and the feedback signal and controlling a feedback loop formed by the decision circuit, the shift register, and the feedback filter based on a monitoring result." As such, the present invention results in the advantage of having a signal processing circuit that prevents pseudo lock of the timing recovery PLL.

It is respectfully submitted that the prior art fails to disclose or suggest at least the combination of elements of the Applicant's invention as set forth in claims 1, 9 and

15, and therefore fails to provide the advantages which are provided by the present application.

AAPA discloses a signal processing circuit 10 including an analog-to-digital converter (ADC) 11, a decision feedback equalizer (DFE) 12, coefficient registers 13 and 14, a PLL phase error detection circuit 15, a timing recovery PLL (TR-PLL) 16, and a control circuit 17.

The ADC 11 samples an analog signal read from a recording medium in accordance with a clock signal CLK supplied from the TR-PLL 16 and converts the analog read signal to a digital read signal. The DFE 12 includes a forward (FW) filter 21, an adder 22, a comparator 23, a shift register 24, a feedback (FB) filter 25, an inverter circuit 26, and switches 27, 28, and 29.

Applicant respectfully submits that each and every element recited within claims 1, 9 and 15 is neither disclosed nor suggested by AAPA. In particular, Applicant submits that the signal processing circuit and the feedback control method as recited in the present application is clearly distinct from that which is disclosed in AAPA. Specifically, it is submitted that AAPA fails to disclose or suggest at least the following elements of the claimed invention.

> Claim 1: "a loop control circuit for monitoring the filtered digital signal and the feedback signal and controlling a feedback loop formed by the decision circuit, the shift register, and the feedback filter based on a monitoring result."
>
> Claim 9: "monitoring the filtered digital signal and the feedback signal; and selecting whether the feedback signal is fed back to the step of generating the addition signal based on a monitoring result."

Claim 15: "determining whether the first phase difference is within a predetermined range; feeding back the feedback signal to the step of generating the addition signal when the first phase difference is within the predetermined range."

As mentioned above, Figure 1 of AAPA merely discloses a control circuit 17 that controls a feedback loop on the basis of only an output signal (DATA) output from a shift register 24, and therefore fails to disclose or suggest a control circuit for controlling a feedback loop on the basis of the filtered digital signal and the feedback signal, and also fails to disclose or suggest the steps of monitoring a filtered digital signal and a feedback signal and selecting whether the feedback signal is fed back to a stop of generating an addition signal based on a monitoring result; of determining whether a first phase difference between a digital signal and a clock signal is within a predetermined range and feeding back a feedback signal to a step of generating an addition signal when the first phase difference is within predetermined range. Therefore, Applicant submits that AAPA fails to disclose or suggest each and every limitation recited within claims 1, 9 and 15.

As for claims 2-4, 6-8, 10-12 and 14, Applicant submits that each of these claims recites subject matter which is neither disclosed nor suggested in the cited prior art. In particular, each of claims 2-4, 6-8, 10-12 and 14 depends from claim 1, 9 and 15, respectively. Therefore, each of these claims incorporates each and every limitation recited within claims 1, 9 and 15, respectively therein. Accordingly, Applicants respectfully submit that each of claims 2-4, 6-8, 10-12 and 14 also recites subject matter that is neither disclosed nor suggested by AAPA, for at least the reasons set forth above with respect to claims 1, 9 and 15.

Claims 5 and 13 were rejected under 35 U.S.C. § 103(a) as being unpatentable over AAPA in view of Kobayashi et al. (US Patent No. 5,963,581, hereinafter "Kobayashi"). AAPA was cited for allegedly disclosing many of the claimed elements of the present invention with the exception of the detection circuit having a plurality of phase comparison gains. Kobayashi was cited for allegedly curing this deficiency.

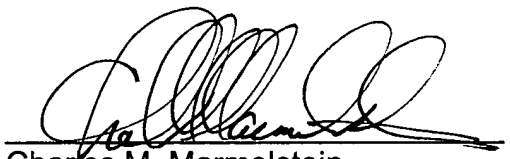
Applicant submits that claims 5 and 13 depend from allowable claims 1 and 9, respectively, these claims are likewise allowable.

In view of the above, Applicant respectfully submits that claims 1-15, each recites subject matter that is neither disclosed nor suggested in the cited prior art. Applicant also submits that the subject matter is more than sufficient to render the claims non-obvious to a person of ordinary skill in the art, and therefore respectfully requests that claims 1-15 be found allowable and that this application be passed to issue.

If for any reason, the Examiner determines that the application is not now in condition for allowance, it is respectfully requested that the Examiner contact the Applicant's undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this application.

In the event this paper has not been timely filed, the Applicants respectfully petition for an appropriate extension of time. Any fees for such an extension, together with any additional fees that may be due with respect to this paper, may be charged to counsel's Deposit Account No. 01-2300, **referencing docket number 108075-09006.**

Respectfully submitted,



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Enclosures:
Petition for Revival (Unintentional) under 37 C.F.R. §1.137(b)
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